

EXHIBIT E

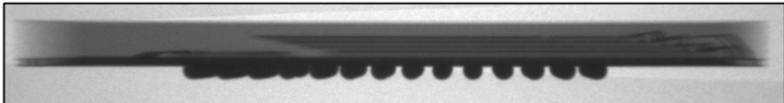
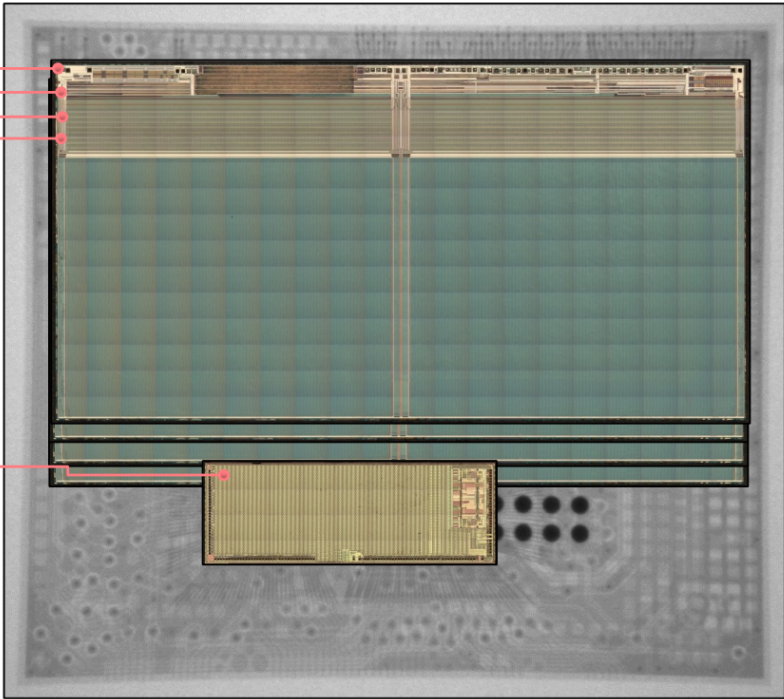
U.S. Patent No. 6,724,241 (“’241 Patent”)

Accused Products

Google products with SanDisk/Toshiba 64L 3D NAND flash chips, including without limitation the Google Pixel 4XL (“Accused Products”), infringe at least Claims 1-3, 6-8, and 11 of the ’241 Patent.

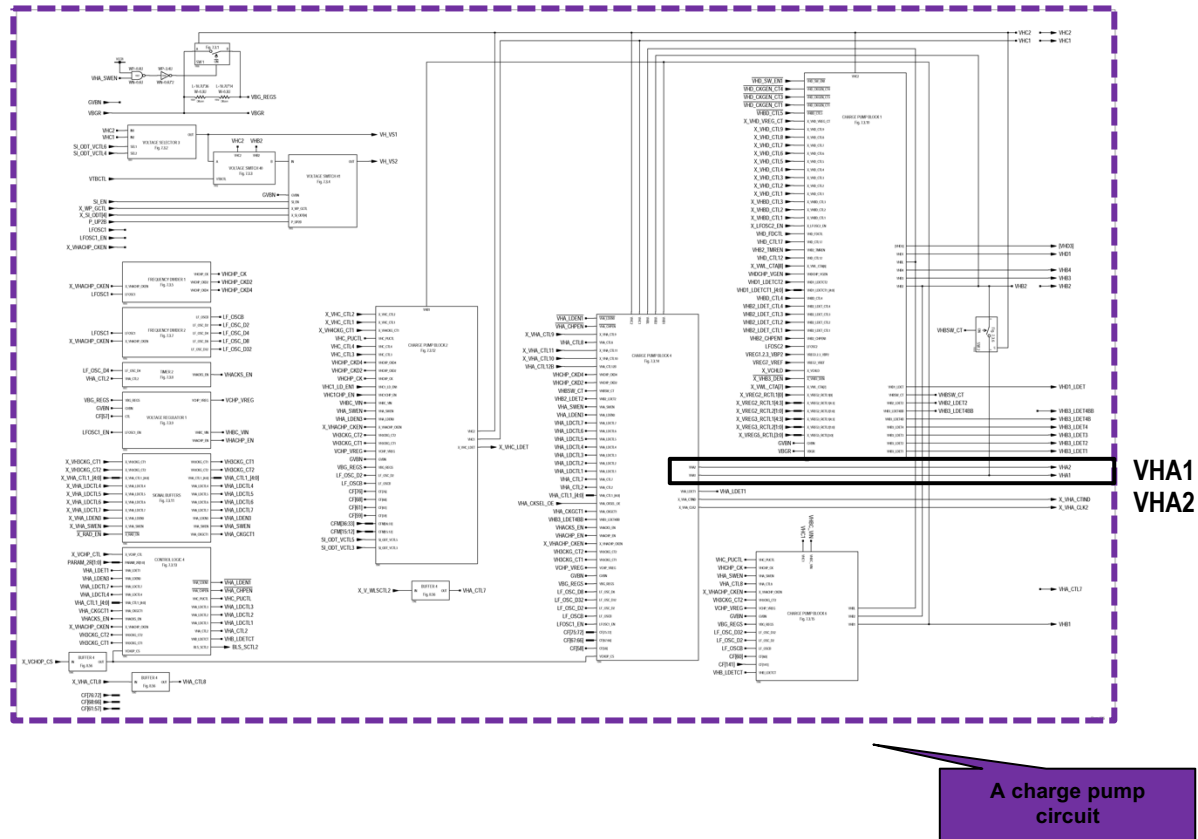
Claim 1

Claim 1	Accused Products
[1pre] 1. A charge pump circuit for generating a charge pump voltage having minimal voltage ripples, comprising:	<p>To the extent the preamble is limiting, each Accused Product includes a charge pump circuit for generating a charge pump voltage having minimal voltage ripples.</p> <p>For example, the Google Pixel 4XL includes the charge pump circuit of the SanDisk/Toshiba 3D NAND flash chip, die identifier FRN1256G.</p> <p><i>See, e.g.:</i></p>

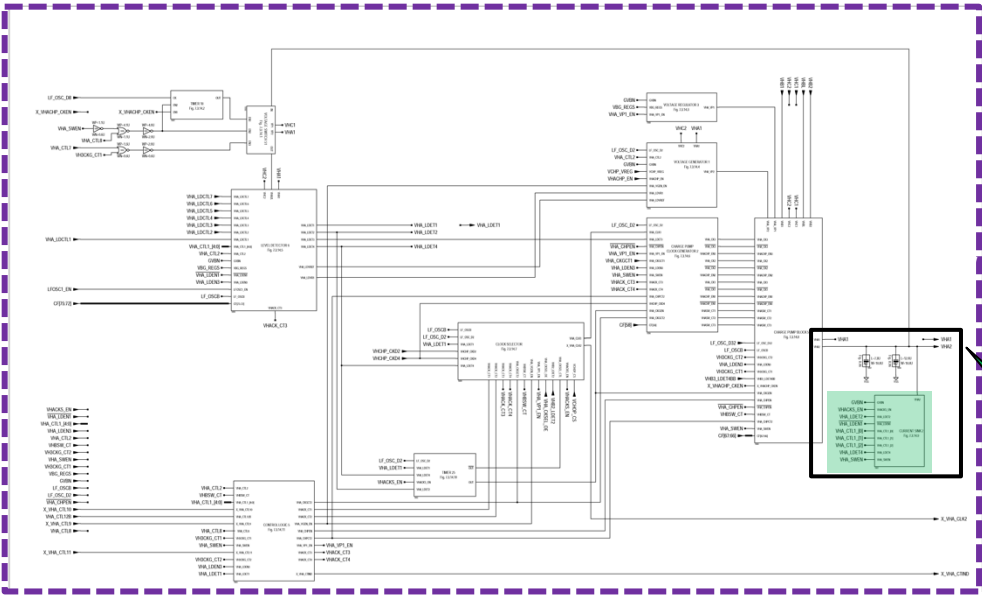
Claim 1	Accused Products
	<div data-bbox="646 269 1010 363"><p>3 - Toshiba #THGAF8T0T43BAIR Multichip Memory - 128 GB 3D TLC NAND Flash, Memory Controller (UFS 2.1) (5-Die Pkg.) Pkg Size: 12.98 x 11.68 mm</p></div> <div data-bbox="646 407 919 487"><p>3.2 - Toshiba #FRN1256G 3D TLC NAND Flash Memory - 32 GB Die Size: 12.13 x 6.26 mm</p></div> <div data-bbox="827 805 1016 883"><p>3.1 - Toshiba #FRZ8 0002 Memory Controller Die Size: 5.24 x 1.83 mm</p></div> <div data-bbox="1100 263 1879 365"></div> <div data-bbox="1100 381 1879 1075"></div> <div data-bbox="655 1036 835 1078"><p>Function: Memory: Non-Volatile</p></div> <div data-bbox="636 1084 1743 1122"><p>Source: TechInsights Deep Dive Teardown, Google Pixel 4 XL G020J ID354397-NDe</p></div>

Claim 1

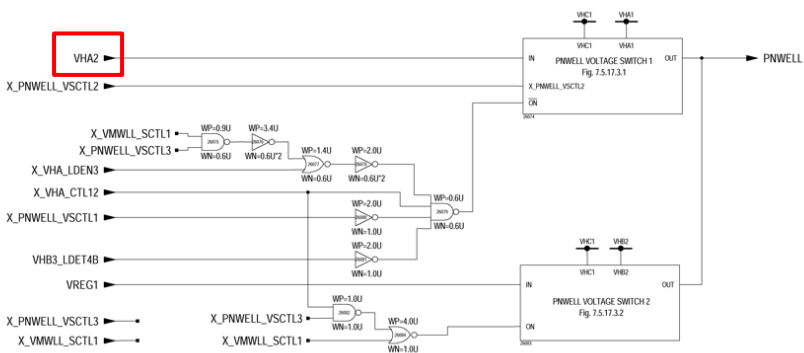
Accused Products

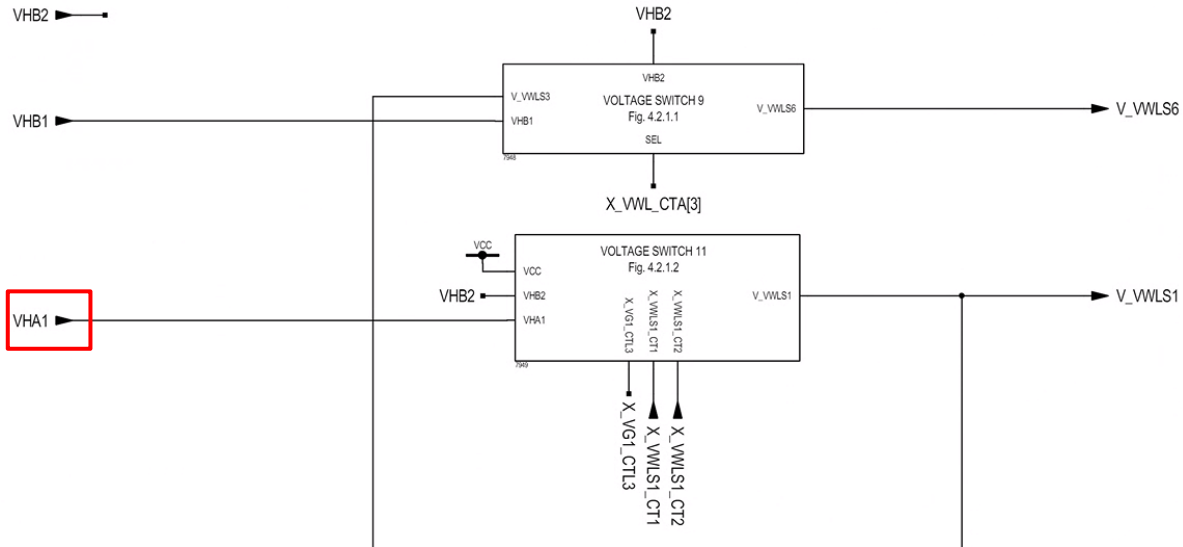


Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3 Charge Pump System

Claim 1	Accused Products
	<div data-bbox="634 316 1610 906"></div> <p data-bbox="634 974 1827 1047">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3 Charge Pump System</p>

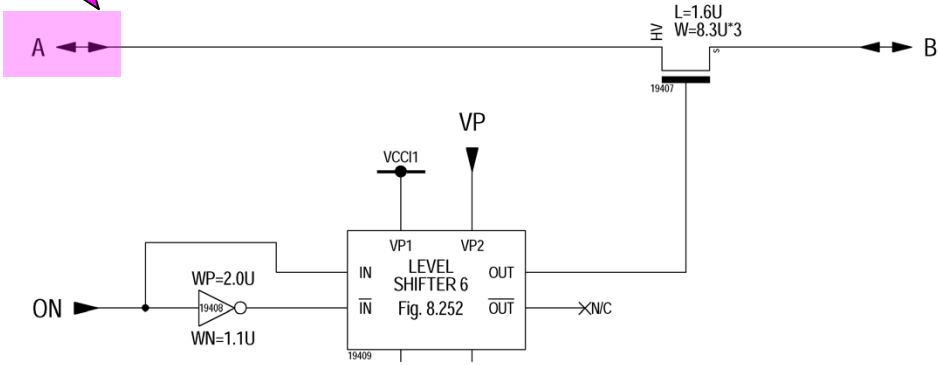
Claim 1	Accused Products
	<div data-bbox="640 267 1606 933"></div> <div data-bbox="1591 310 1871 418" style="background-color: red; color: black; padding: 5px;"><p>for generating a charge pump voltage (VHA1, VHA2)</p></div> <div data-bbox="1612 483 1850 581" style="background-color: white; color: black; padding: 5px;"><p>VHA1 and VHA2 are driven by the same pumping circuit</p></div> <div data-bbox="1625 651 1839 716" style="background-color: purple; color: white; padding: 5px;"><p>A charge pump circuit</p></div>
<p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5</p>	

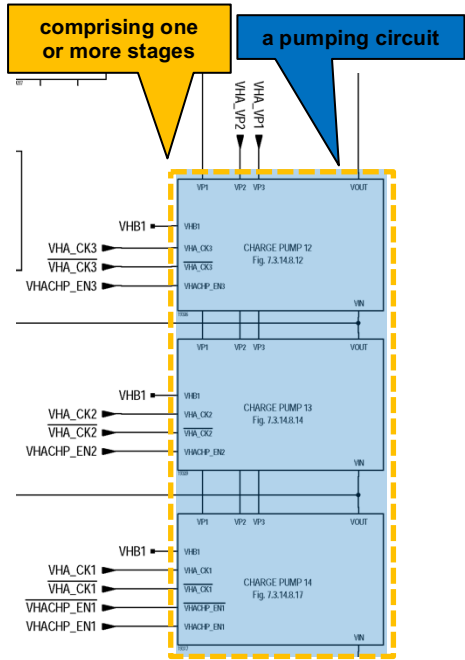
Claim 1	Accused Products
	<p data-bbox="674 300 1241 362">Charge pump output voltage VHA2 is provided to high voltage switches to selectively drive PNWELL.</p>  <p data-bbox="632 829 1829 901">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.5.17.3 PNWELL Voltage Selector</p>

Claim 1	Accused Products
	<p>Charge pump output voltage VHA1 is provided to high voltage switches to selectively drive wordline circuits.</p>  <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 4.2.1 Wordline Voltage Switch Block 1</p>
<p>[1a] a) a pumping circuit comprising one or more stages operable to receive a supply voltage and generate a selected one of a plurality of pump voltages;</p>	<p>Each Accused Product includes a pumping circuit comprising one or more stages operable to receive a supply voltage and generate a selected one of a plurality of pump voltages.</p> <p>For example, in the pumping circuit, 1, 2, or 3 main stages can be enabled for operation. Supply voltage can be selected from external VCC or internally generated pumped voltages VHBL or VHB1. VHA2 is provided to a level detector which suspends pump clocks when a desired level is reached. VHA2 is scaled by a fixed ratio voltage divider (Voltage Divider 2). It is then compared (using Amplifier 12) to an adjustable reference voltage (generated by Reference Voltage Regulator). A 4-bit digital code CF(75:72) adjusts the output reference voltage by shorting out</p>

Claim 1	Accused Products
	<p>resistors in a resistor divider, thereby providing programmable pump output voltage levels on VHA1 and VHA2. A comparator (Amplifier 12) compares the scaled VHA2 to the programmable reference voltage. If the scaled VHA2 exceeds the programmable reference voltage, output VHA_LDET3 transitions from 1 to 0 to stop further pumping. VHA_CK2 and VHA_CK2* drive the middle stage of the pumping circuit. VHA_PH2 non-overlapping clocks drive Charge Pump 13. When VHA_PH2 clocks are suspended the pump stops operating so that VHA1 is limited to the voltage set by the level detector.</p> <p><i>See, e.g.:</i></p>

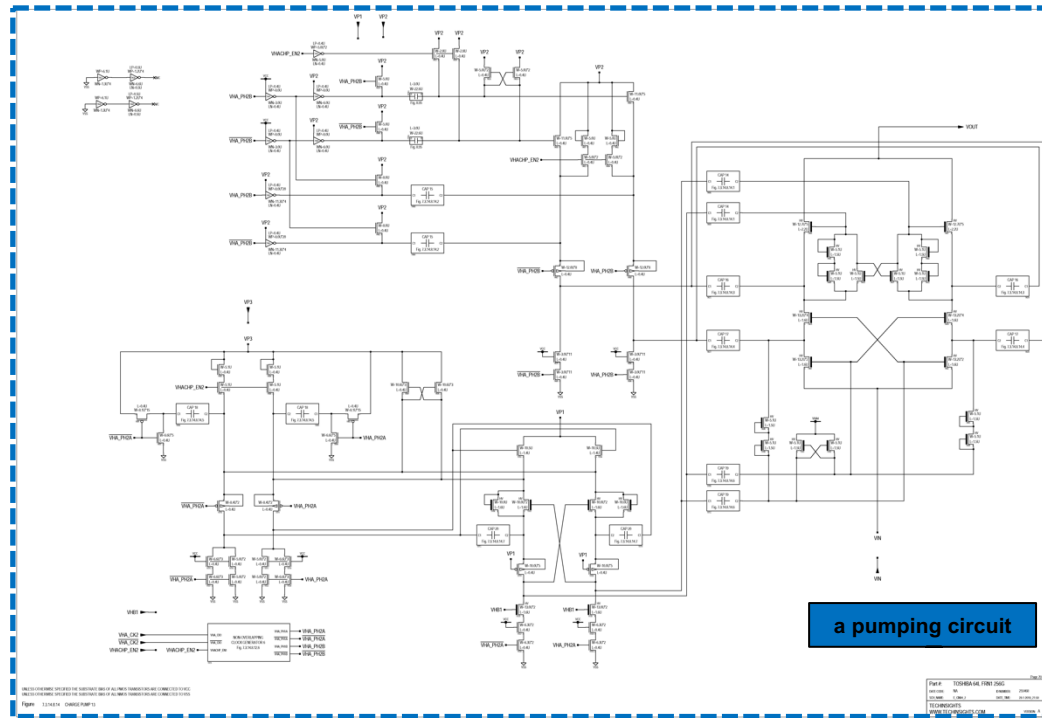
[illegible]

Claim 1	Accused Products
	<p data-bbox="632 266 963 326">operable to receive a supply voltage (VCC)</p>  <p data-bbox="632 792 1829 867">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.6 Voltage Switch 55</p>

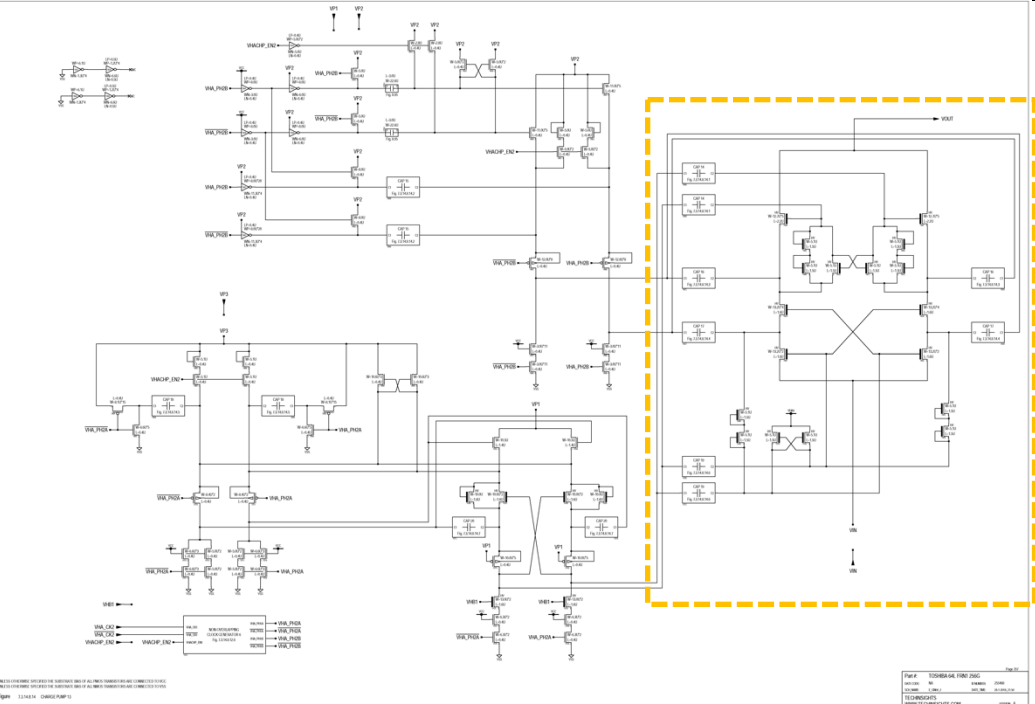
Claim 1	Accused Products
	 <p>The diagram illustrates three charge pumps, labeled CHARGE PUMP 12, CHARGE PUMP 13, and CHARGE PUMP 14, arranged vertically. Each pump is enclosed in a dashed yellow box, indicating they are part of a single functional block. Above the pumps, two callout boxes are present: a yellow one labeled 'comprising one or more stages' pointing to the input side of the pumps, and a blue one labeled 'a pumping circuit' pointing to the output side. Each pump has multiple input pins on the left: VHB1, VHA_CK1, VHA_CK2, VHA_CK3, VHA_OK1, VHA_OK2, VHA_OK3, VHA_CHP_EN1, VHA_CHP_EN2, and VHA_CHP_EN3. The output of each pump is labeled VOUT. The pumps are connected to a common ground line labeled VN. The diagram shows that each pump has multiple stages, with the output of one stage feeding into the next stage of the same pump. The pumps are connected to a common output line labeled VOUT.</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5</p>

Claim 1

Accused Products

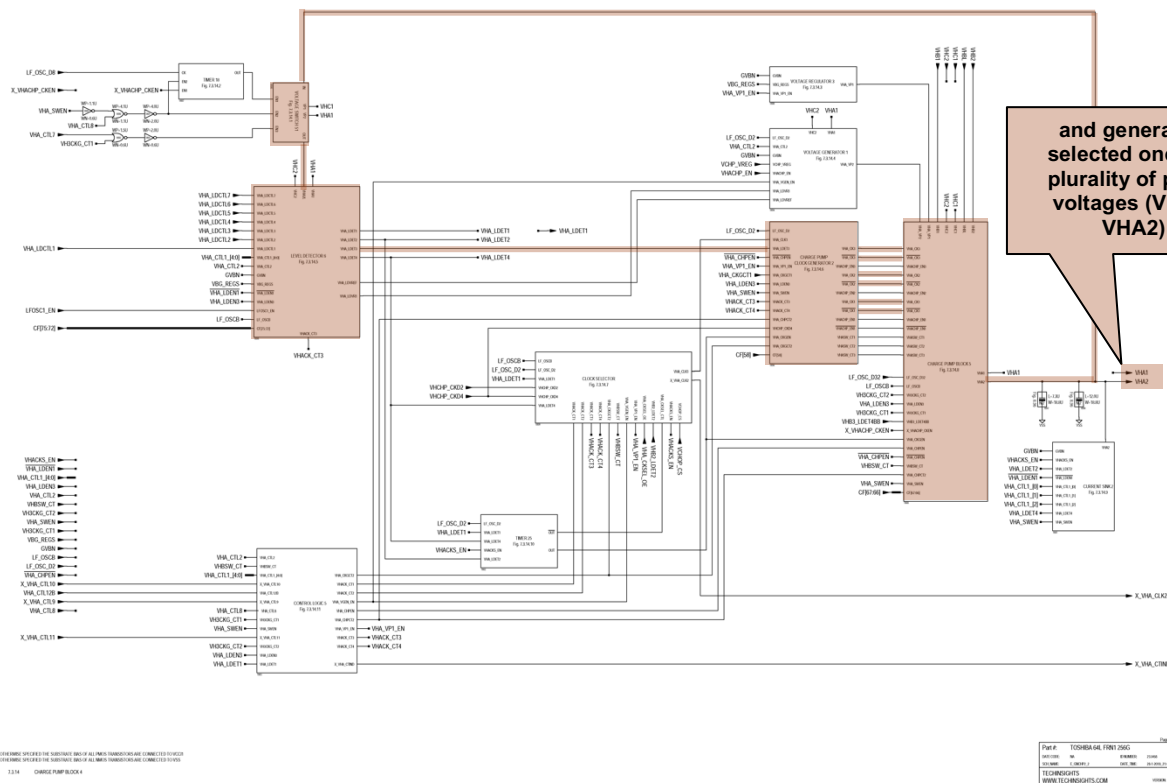


Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.14 Charge Pump 13

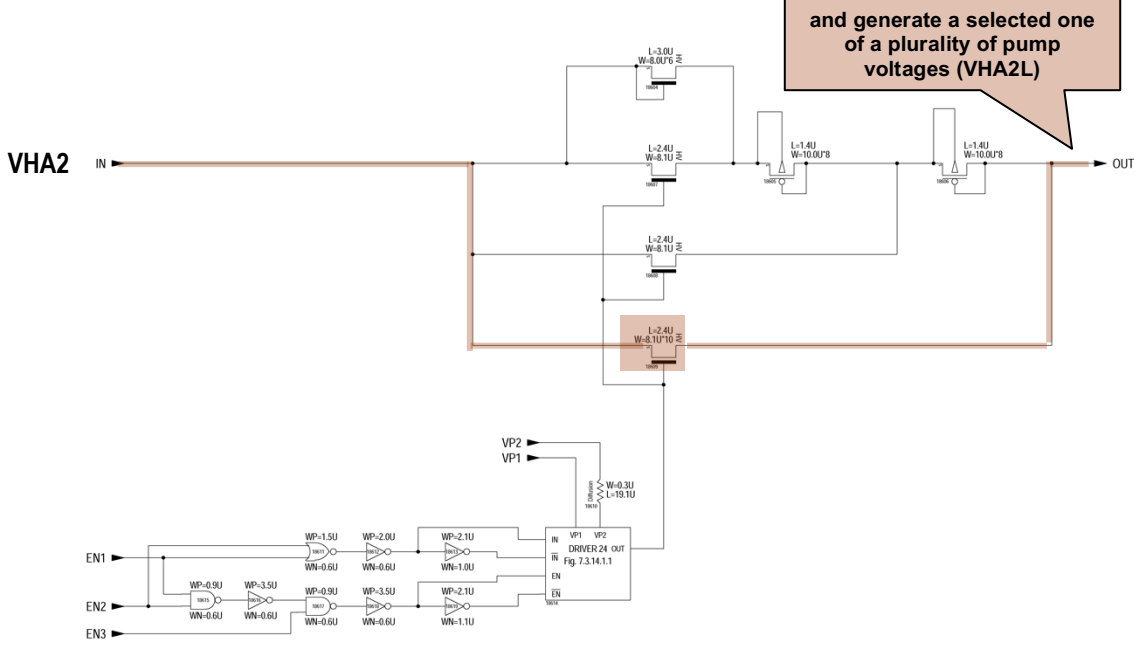
Claim 1	Accused Products
	 <p>comprising one or more stages</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.14 Charge Pump 13</p>

Claim 1

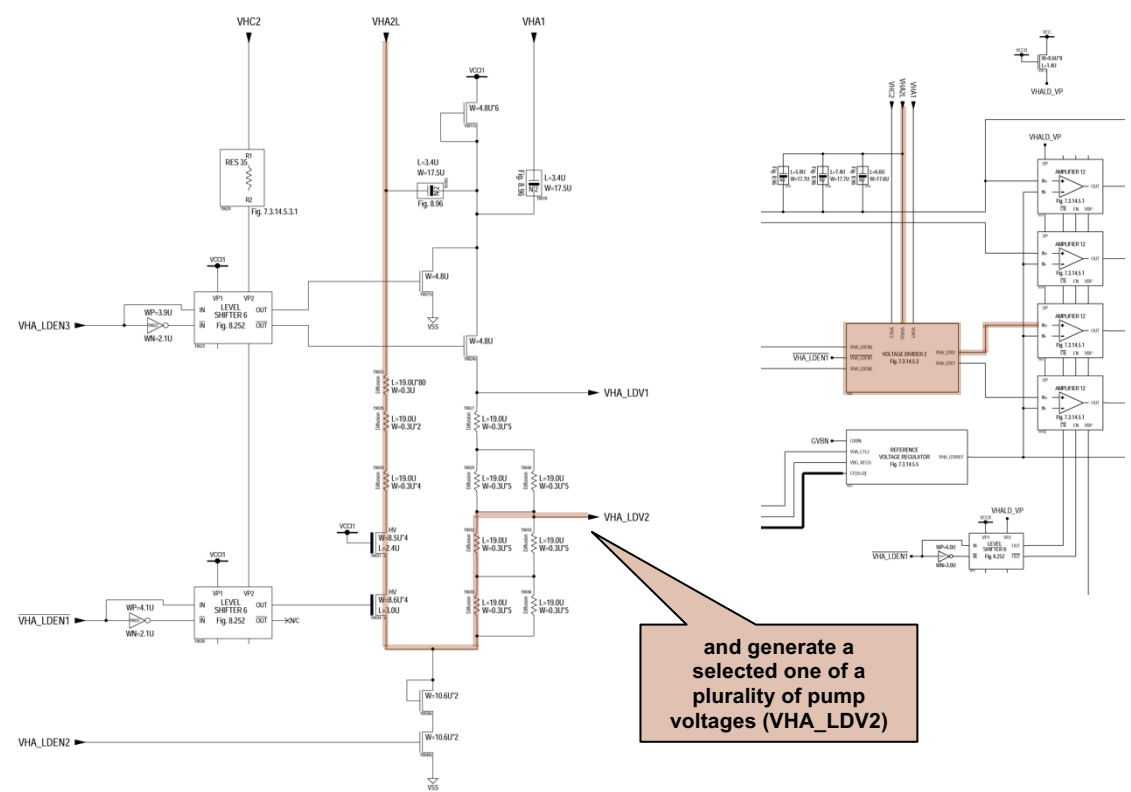
Accused Products



Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14 Charge Pump Block 4

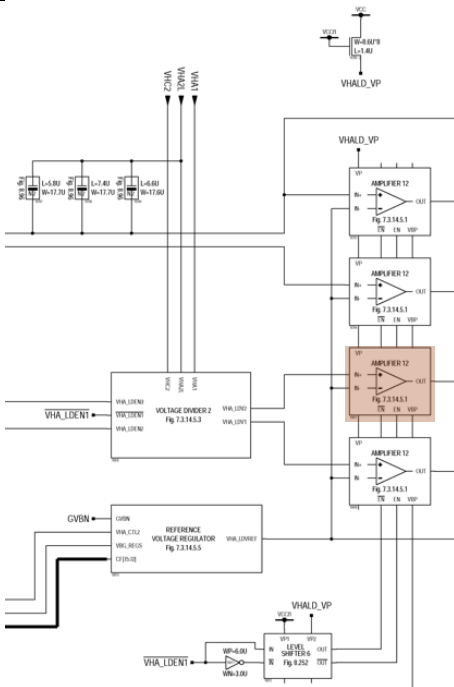
Claim 1	Accused Products
	 <p>The diagram shows a circuit for a voltage switch (VHA2). It includes an input (IN) and an output (OUT). The circuit features several transistors (MOSFETs) and capacitors. A callout box points to a specific transistor with the text: "and generate a selected one of a plurality of pump voltages (VHA2L)".</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.1 Voltage Switch 51</p>

Claim 1	Accused Products

Claim 1	Accused Products
	 <p>and generate a selected one of a plurality of pump voltages (VHA_LDV2)</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5.3 Voltage Divider 2; Figure 7.3.14.5 Level Detector 6</p>

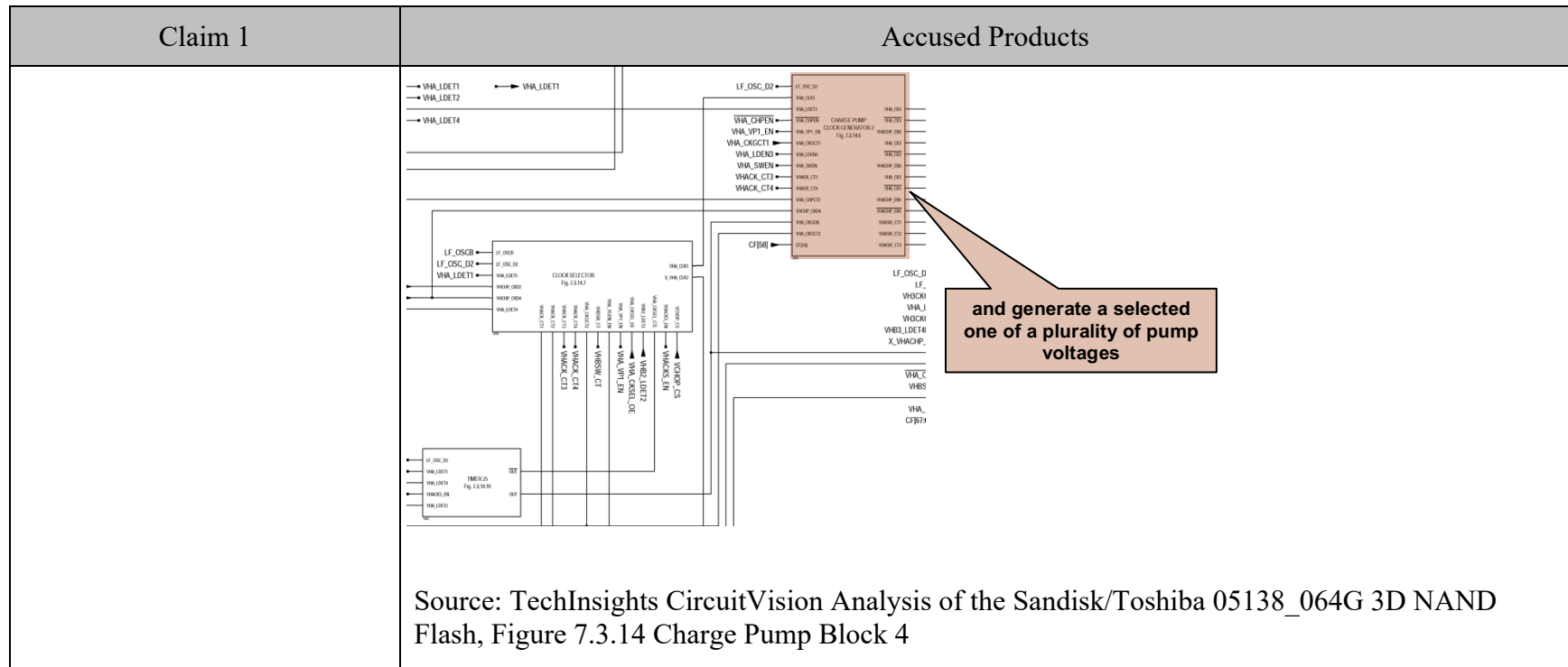
Claim 1	Accused Products
	<p>The circuit diagram shows a level detector for a 3D NAND flash. It includes a voltage divider (Fig. 7.3.14.5.3) connected to VHA_LDREF and VHA_LDREFN. A reference voltage regulator (Fig. 7.3.14.5.5) provides a reference voltage (VHA_LDREF). The output of the voltage divider is compared against the reference voltage using four comparators (AMPLIFIER 12, Fig. 7.3.14.5.1). The outputs of these comparators are used to generate a plurality of pump voltages (VHA_LDVP).</p> <p>and generate a selected one of a plurality of pump voltages (VHA_LDVP)</p>
	Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6

[illegible]

Claim 1	Accused Products
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>

[illegible]

Claim 1	Accused Products
	<p>VHA_LDET3 = 1 Disables VHA_CK2 pump clock to 1 level</p> <p>VHA_CK2 = 1 VHA_CK2* = 0</p> <p>and generate a selected one of a plurality of pump voltages</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.6 Charge Pump Clock Generator 2</p>



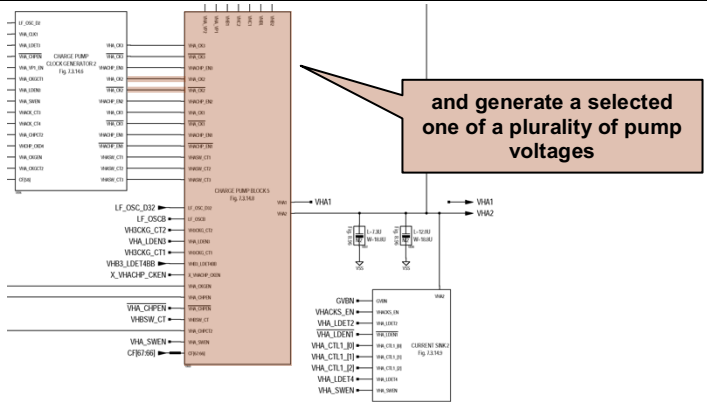
Claim 1

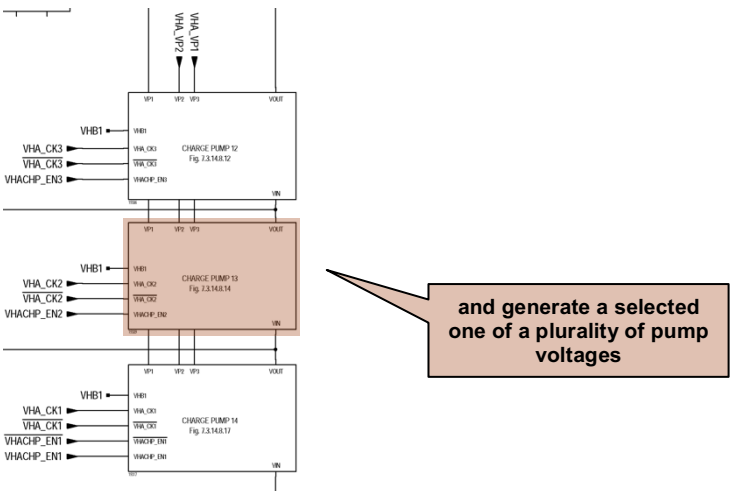
Accused Products

and generate a selected one of a plurality of pump voltages

a pumping circuit

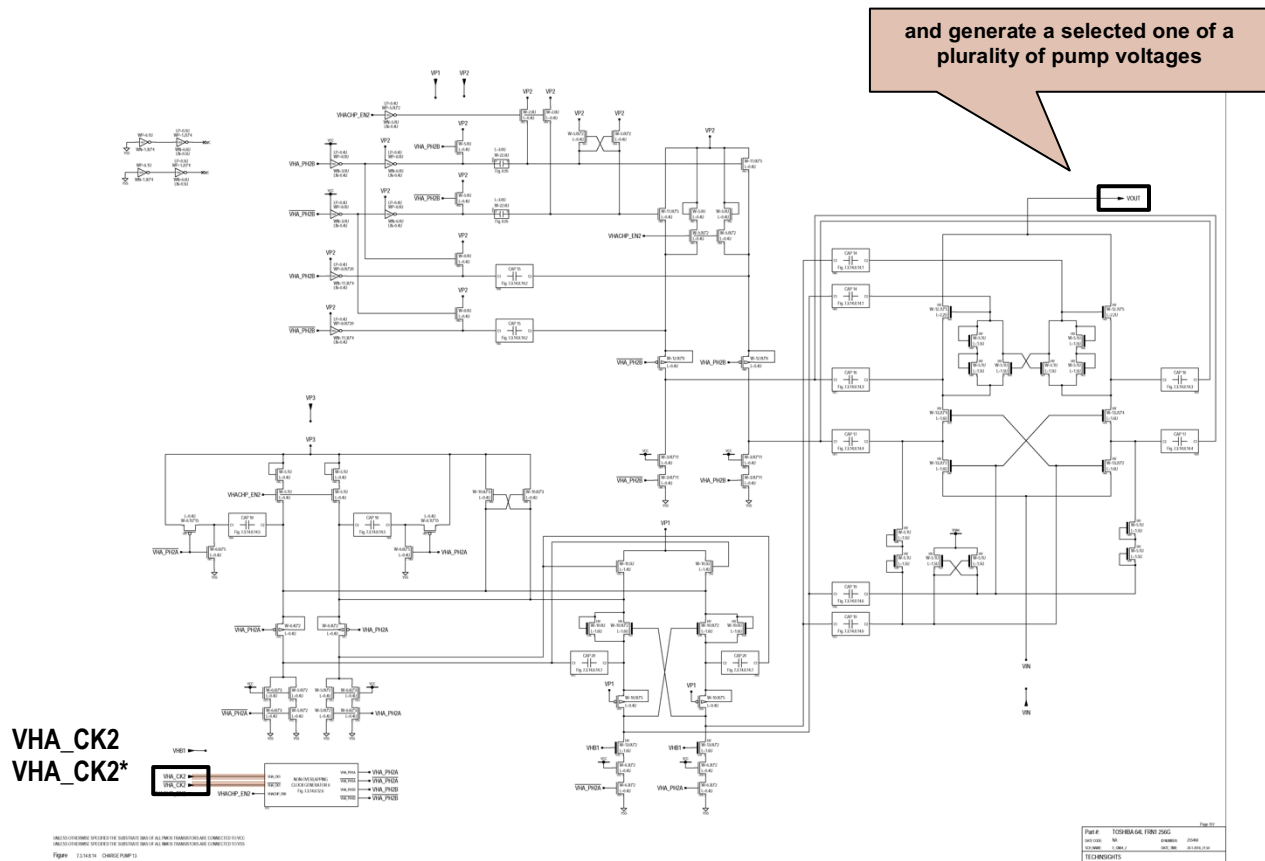
Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5

Claim 1	Accused Products
	 <p>The diagram illustrates a Charge Pump Block (Fig. 13.14.3) with multiple input and output pins. Inputs include VDD, VDD1, VDD2, VDD3, VDD4, VDD5, VDD6, VDD7, VDD8, VDD9, VDD10, VDD11, VDD12, VDD13, VDD14, VDD15, VDD16, VDD17, VDD18, VDD19, VDD20, VDD21, VDD22, VDD23, VDD24, VDD25, VDD26, VDD27, VDD28, VDD29, VDD30, VDD31, VDD32, VDD33, VDD34, VDD35, VDD36, VDD37, VDD38, VDD39, VDD40, VDD41, VDD42, VDD43, VDD44, VDD45, VDD46, VDD47, VDD48, VDD49, VDD50, VDD51, VDD52, VDD53, VDD54, VDD55, VDD56, VDD57, VDD58, VDD59, VDD60, VDD61, VDD62, VDD63, VDD64, VDD65, VDD66, VDD67, VDD68, VDD69, VDD70, VDD71, VDD72, VDD73, VDD74, VDD75, VDD76, VDD77, VDD78, VDD79, VDD80, VDD81, VDD82, VDD83, VDD84, VDD85, VDD86, VDD87, VDD88, VDD89, VDD90, VDD91, VDD92, VDD93, VDD94, VDD95, VDD96, VDD97, VDD98, VDD99, VDD100. Outputs include VDD101, VDD102, VDD103, VDD104, VDD105, VDD106, VDD107, VDD108, VDD109, VDD110, VDD111, VDD112, VDD113, VDD114, VDD115, VDD116, VDD117, VDD118, VDD119, VDD120, VDD121, VDD122, VDD123, VDD124, VDD125, VDD126, VDD127, VDD128, VDD129, VDD130, VDD131, VDD132, VDD133, VDD134, VDD135, VDD136, VDD137, VDD138, VDD139, VDD140, VDD141, VDD142, VDD143, VDD144, VDD145, VDD146, VDD147, VDD148, VDD149, VDD150, VDD151, VDD152, VDD153, VDD154, VDD155, VDD156, VDD157, VDD158, VDD159, VDD160, VDD161, VDD162, VDD163, VDD164, VDD165, VDD166, VDD167, VDD168, VDD169, VDD170, VDD171, VDD172, VDD173, VDD174, VDD175, VDD176, VDD177, VDD178, VDD179, VDD180, VDD181, VDD182, VDD183, VDD184, VDD185, VDD186, VDD187, VDD188, VDD189, VDD190, VDD191, VDD192, VDD193, VDD194, VDD195, VDD196, VDD197, VDD198, VDD199, VDD200. Internal components include capacitors (C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100), transistors (M1, M2, M3, M4, M5, M6, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16, M17, M18, M19, M20, M21, M22, M23, M24, M25, M26, M27, M28, M29, M30, M31, M32, M33, M34, M35, M36, M37, M38, M39, M40, M41, M42, M43, M44, M45, M46, M47, M48, M49, M50, M51, M52, M53, M54, M55, M56, M57, M58, M59, M60, M61, M62, M63, M64, M65, M66, M67, M68, M69, M70, M71, M72, M73, M74, M75, M76, M77, M78, M79, M80, M81, M82, M83, M84, M85, M86, M87, M88, M89, M90, M91, M92, M93, M94, M95, M96, M97, M98, M99, M100), and other components (U1, U2, U3, U4, U5, U6, U7, U8, U9, U10, U11, U12, U13, U14, U15, U16, U17, U18, U19, U20, U21, U22, U23, U24, U25, U26, U27, U28, U29, U30, U31, U32, U33, U34, U35, U36, U37, U38, U39, U40, U41, U42, U43, U44, U45, U46, U47, U48, U49, U50, U51, U52, U53, U54, U55, U56, U57, U58, U59, U60, U61, U62, U63, U64, U65, U66, U67, U68, U69, U70, U71, U72, U73, U74, U75, U76, U77, U78, U79, U80, U81, U82, U83, U84, U85, U86, U87, U88, U89, U90, U91, U92, U93, U94, U95, U96, U97, U98, U99, U100). A callout box points to the output stage with the text: 'and generate a selected one of a plurality of pump voltages'.</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14 Charge Pump Block 4</p>

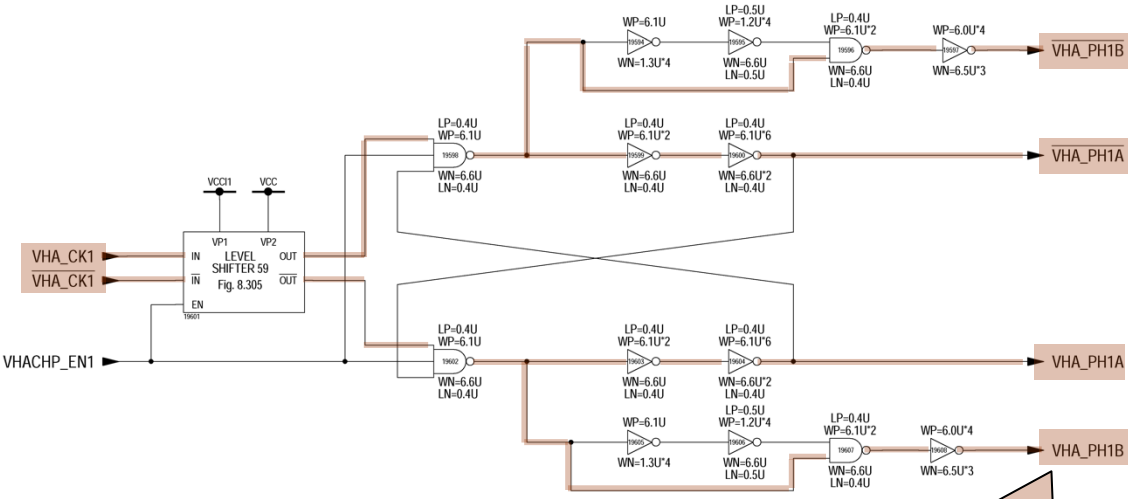
Claim 1	Accused Products
	 <p>and generate a selected one of a plurality of pump voltages</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5</p>

Claim 1

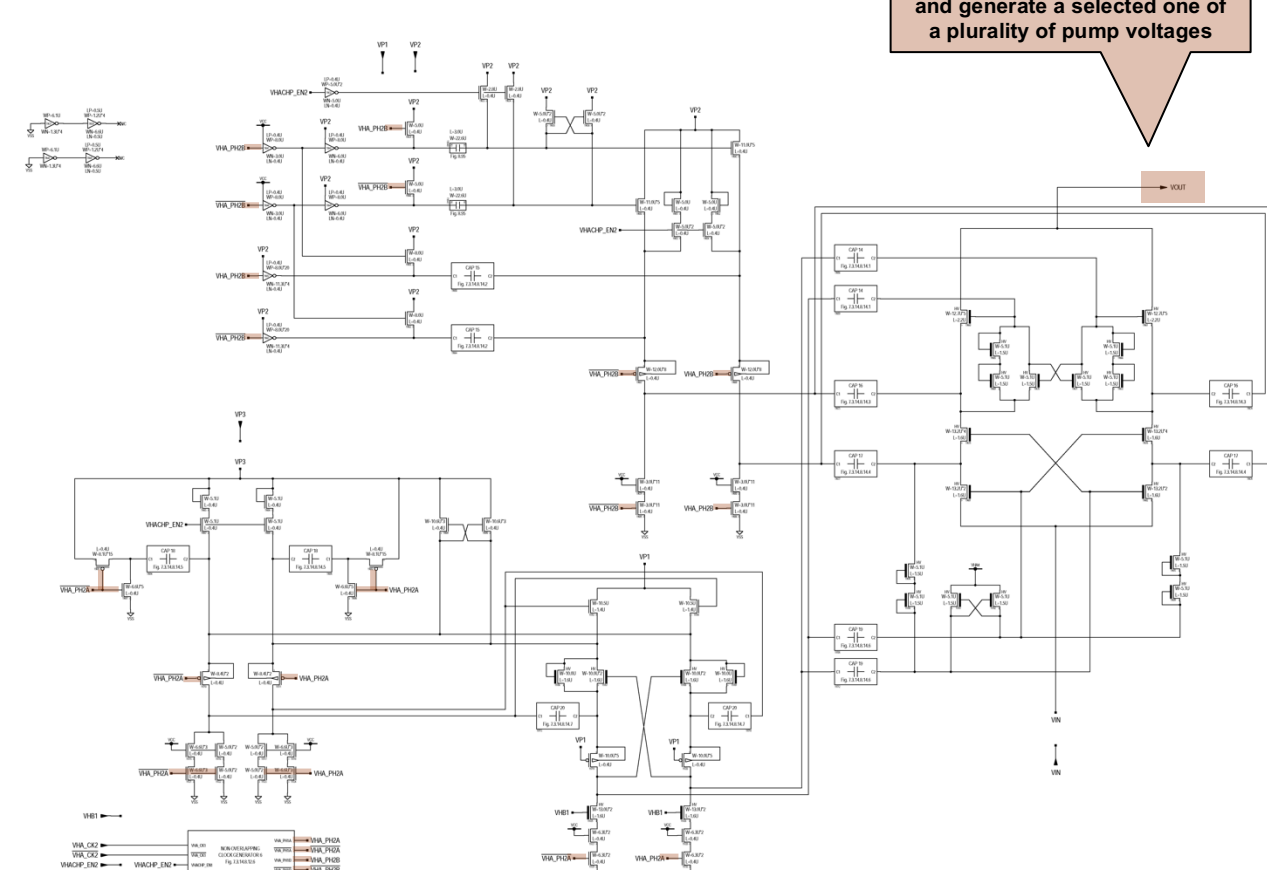
Accused Products



Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.14 Charge Pump 13

Claim 1	Accused Products
	<div data-bbox="636 355 758 417"> <p>VHA_CK2 VHA_CK2*</p> </div> <div data-bbox="1629 293 1766 417"> <p>VHA_PH2A VHA_PH2A* VHA_PH2B VHA_PH2B*</p> </div>  <div data-bbox="1533 951 1887 1013"> <p>and generate a selected one of a plurality of pump voltages</p> </div> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.12.6 Non-Overlapping Clock Generator 6</p>

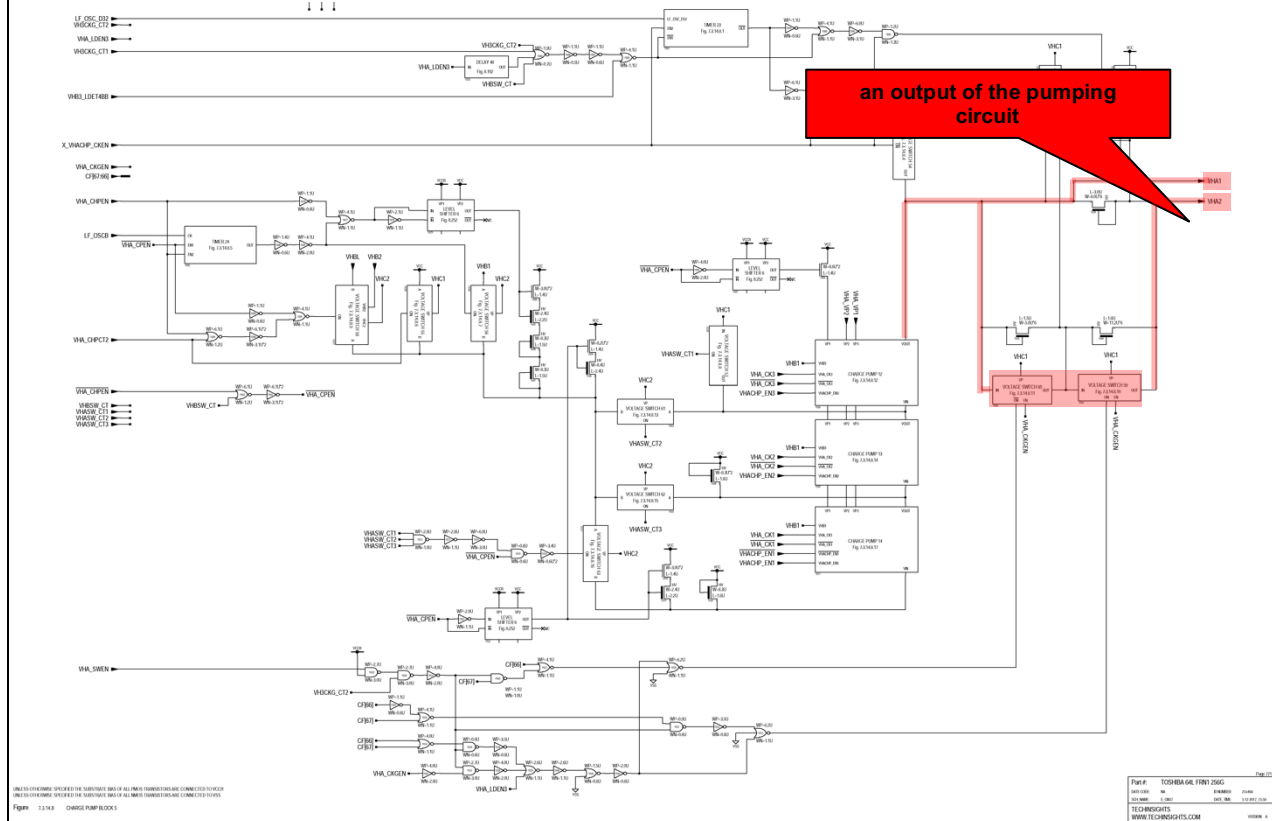
Claim 1	Accused Products

Claim 1	Accused Products
	<div data-bbox="1507 279 1871 441" style="border: 1px solid black; padding: 5px; margin-bottom: 10px;"> <p>and generate a selected one of a plurality of pump voltages</p> </div>  <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.14 Charge Pump 13</p>

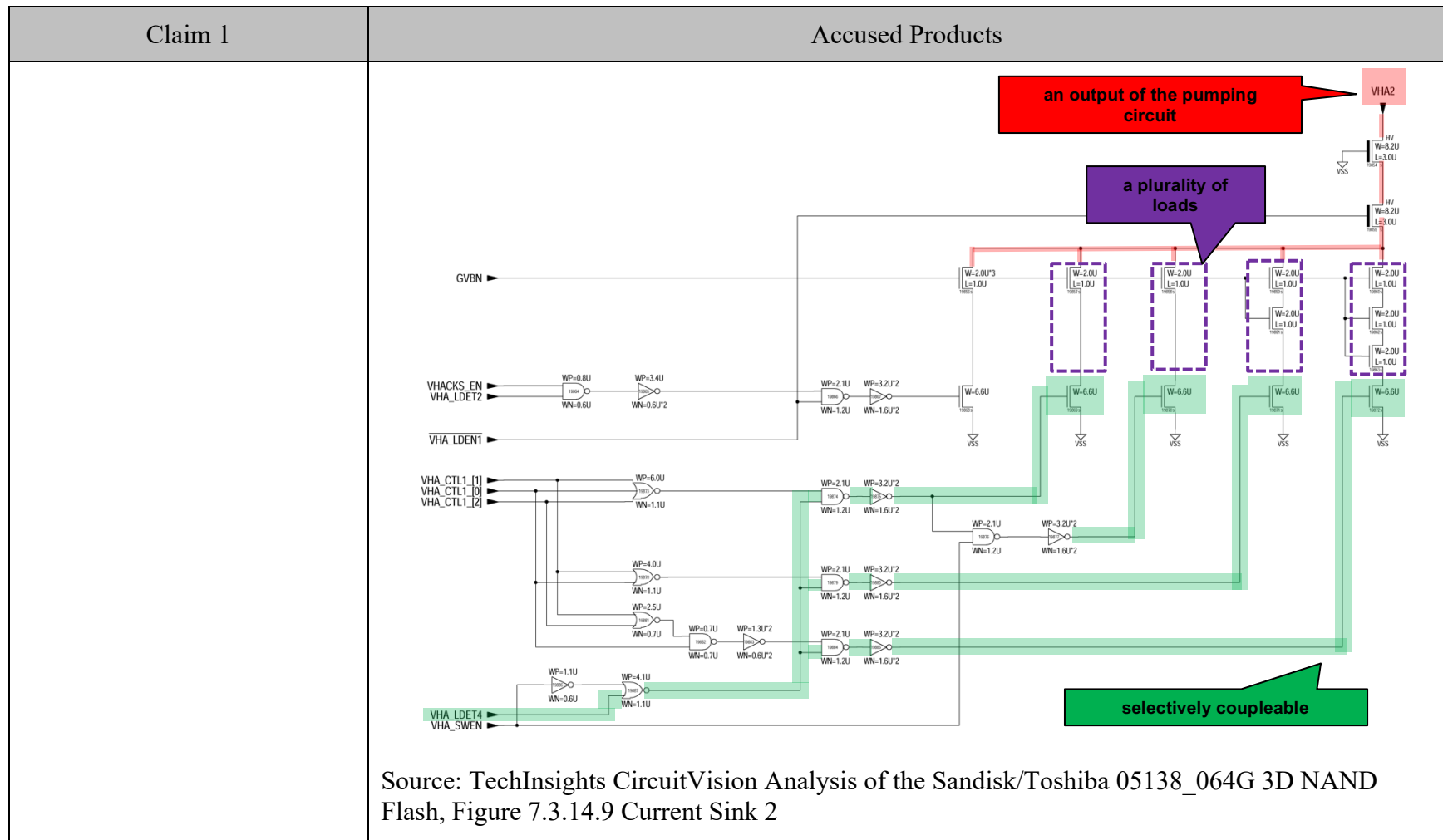
<p>Claim 1</p>	<p>Accused Products</p>
<p>[1b] b) a plurality of loads selectively coupleable to an output of the pumping circuit, each load associated with a specific pump voltage; and</p>	<p>Each Accused Product includes a plurality of loads selectively coupleable to an output of the pumping circuit, each load associated with a specific pump voltage.</p> <p>For example, VHA2 is an output of the pumping circuit. A plurality of loads (contained within Current Sink 2) can be selectively coupled to an output of the pumping circuit (for example VHA2). VHA2 is connected to pumping circuit output VHA1 through Voltage Switches 59 and 60. VHA1 is connected to wordline decoders during read or program operations. Read, program and erase operations require different voltages. Each load is associated with a specific pump voltage to carry out these functions.</p> <p>See, e.g.:</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14 Charge Pump Block 4</p>

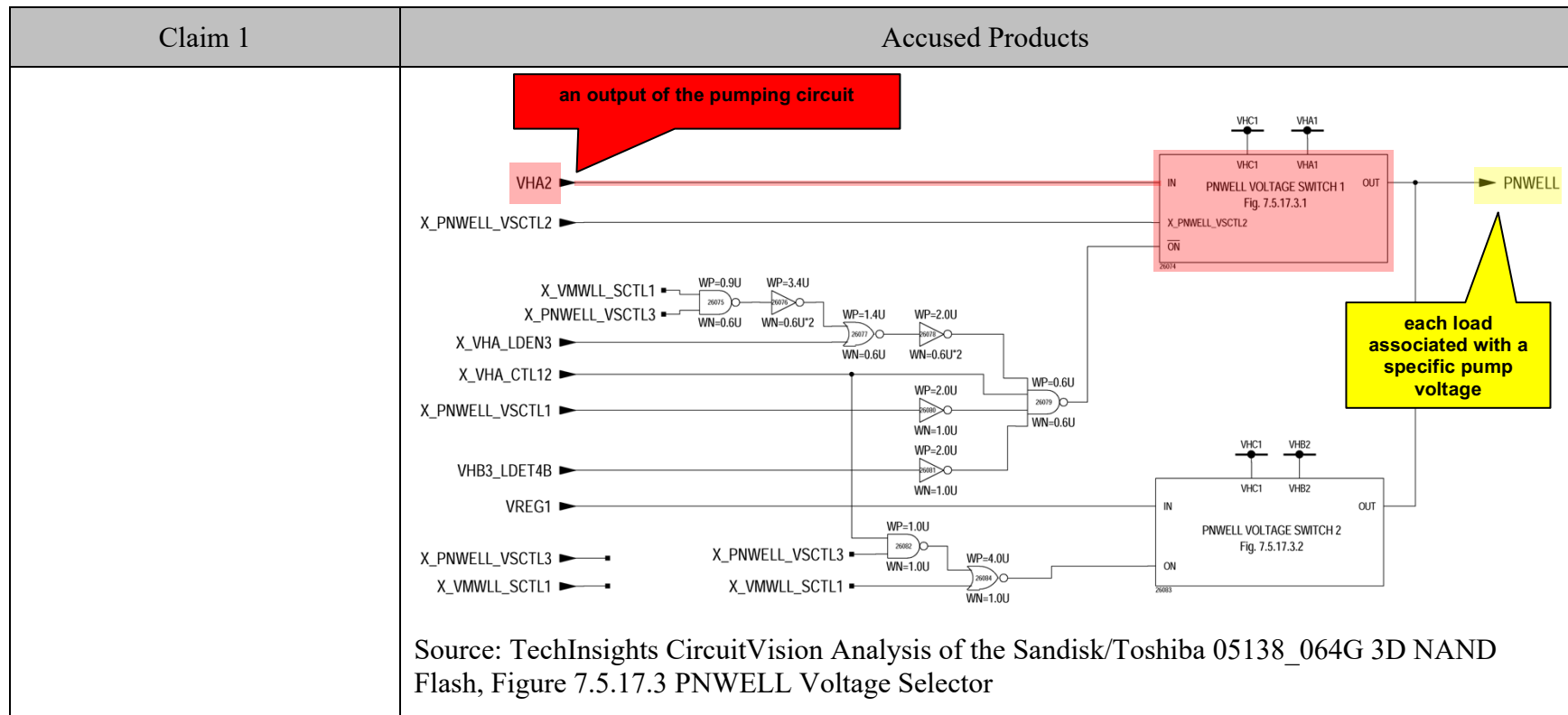
Claim 1

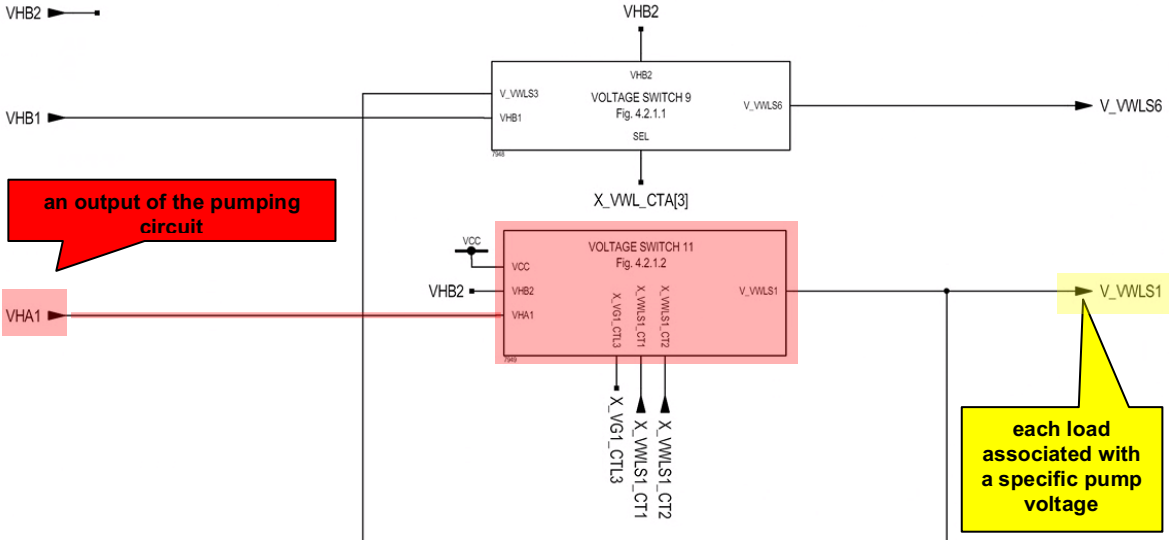
Accused Products



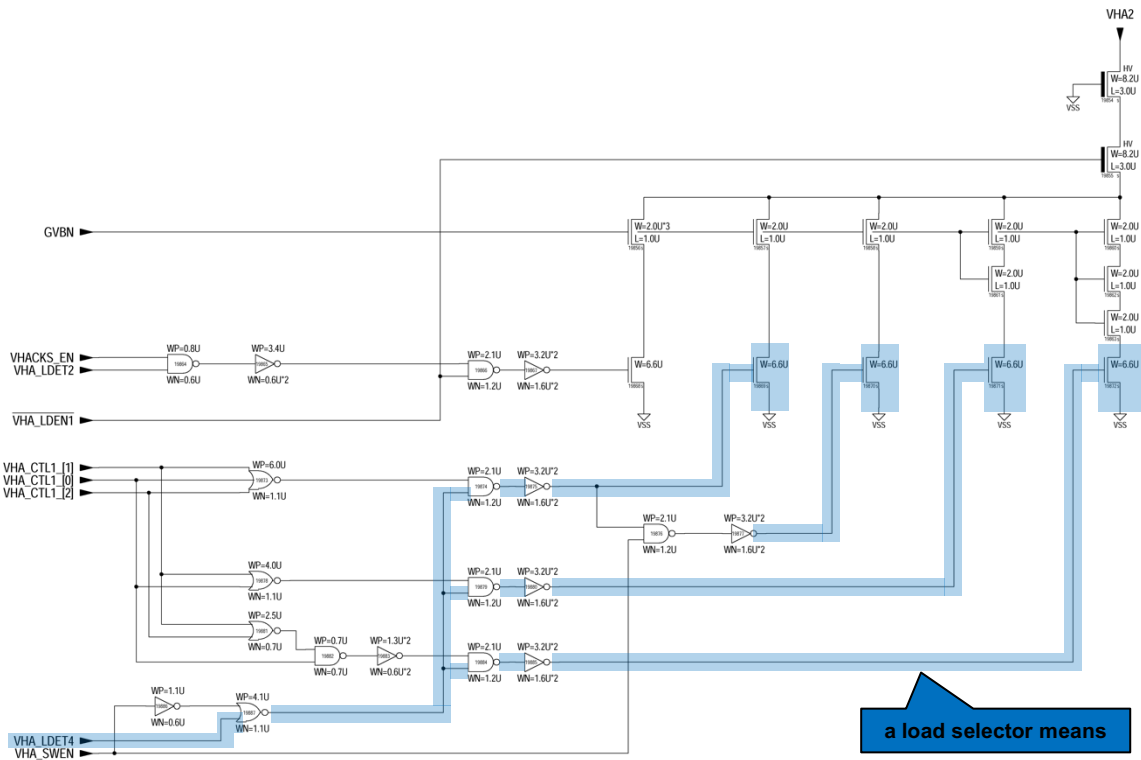
Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5

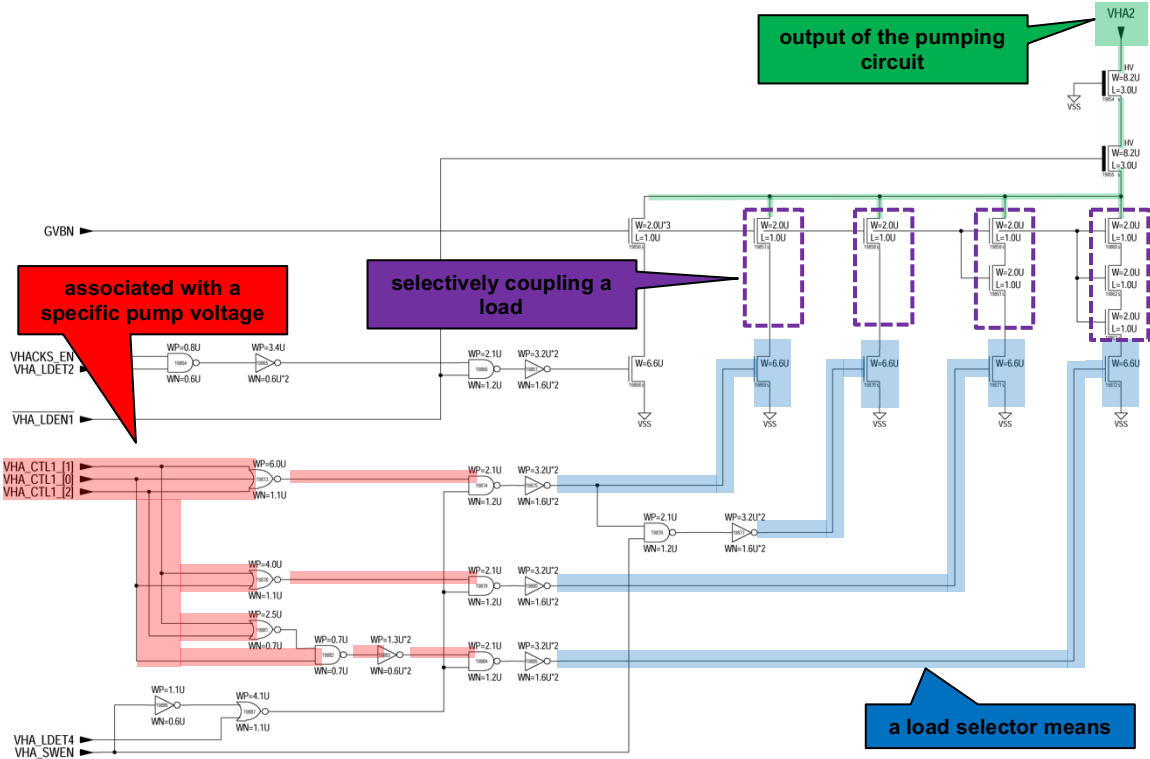




Claim 1	Accused Products
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 4.2.1 Wordline Voltage Switch Block 1</p>
<p>[1c] c) a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit.</p>	<p>Each Accused Product includes a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit.</p> <p>For example, the highlighted transistors below and their respective gate control signals form a load selector means. The output signal VHA_LDET4 from Level Detector 6 forms part of the load selector means. For example, the gate control signals are generated in part by a charge pump control signal (VHA_CTL1). This 3 bit value selectively couples a load associated with a specific pump voltage.</p> <p><i>See, e.g.:</i></p>

[illegible]

Claim 1	Accused Products
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.9 Current Sink 2</p>

Claim 1	Accused Products
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.9 Current Sink 2</p>

Claim 2

Claim 2	Accused Products
2. The charge pump circuit of claim 1, wherein the load selector means includes a	To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 1, wherein the load selector means includes a target output pump selector for shutting down

Claim 2	Accused Products
<p>target output pump selector for shutting down the variable charge pump circuit when the target output pump voltage (Vcfra) is greater than or equal to a reference voltage (Vref).</p>	<p>the variable charge pump circuit when the target output pump voltage (Vcfra) is greater than or equal to a reference voltage (Vref).</p> <p>For example, VHA2 is provided to a level detector which suspends pump clocks when a desired level is reached. VHA2 is scaled by a fixed ratio voltage divider (Voltage Divider 2). It is then compared (using Amplifier 12) to an adjustable reference voltage (generated by Reference Voltage Regulator). A 4-bit digital code CF(75:72) adjusts the output reference voltage by shorting out resistors in a resistor divider, thereby providing programmable pump output voltage levels on VHA1 and VHA2. A comparator (Amplifier 12) compares the scaled VHA2 to the programmable reference voltage. If the scaled VHA2 exceeds the programmable reference voltage, output VHA_LDET3 transitions from 1 to 0 to stop further pumping.</p> <p><i>See evidence and explanation for claim element [1a], supra.</i></p>

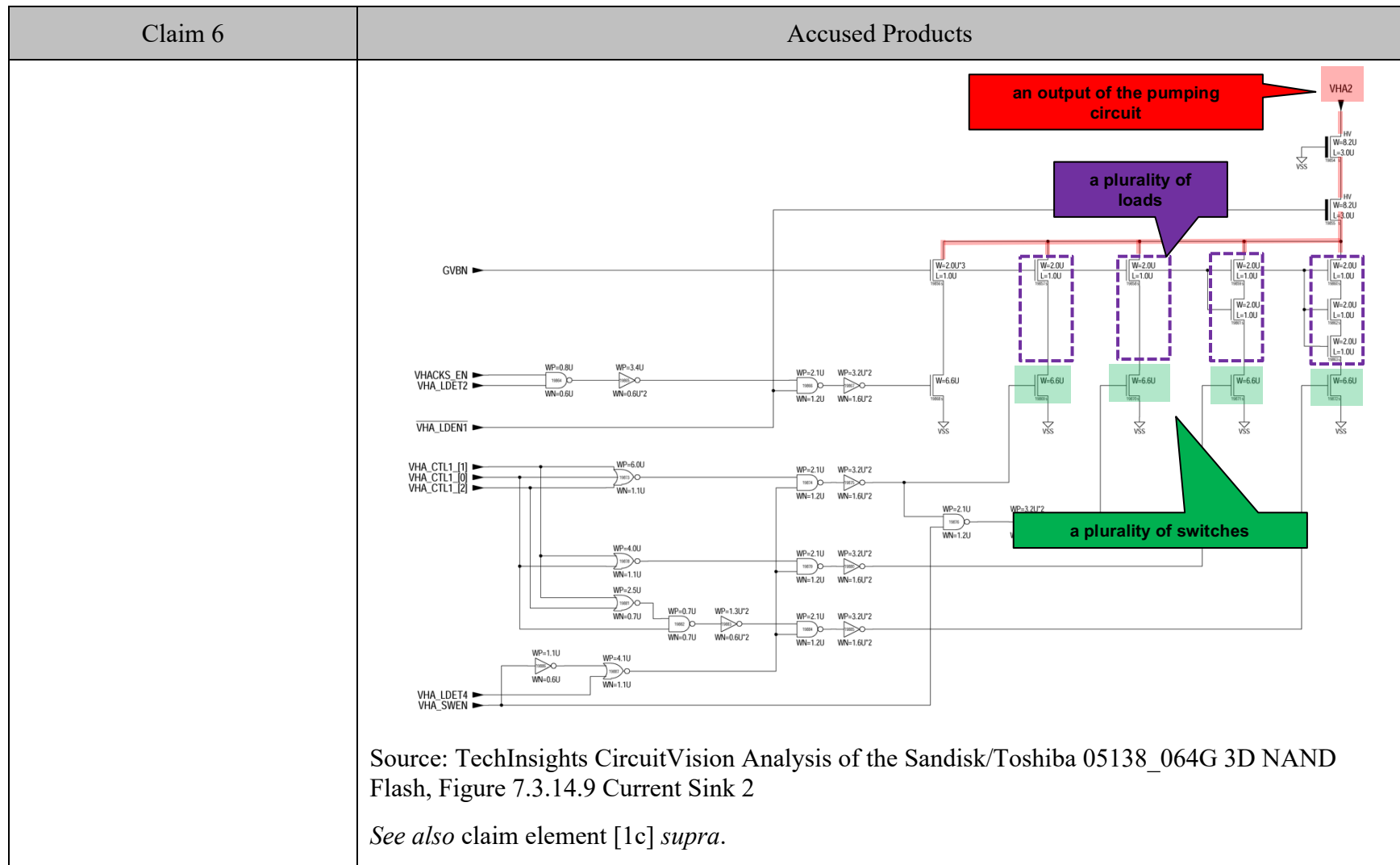
Claim 3

Claim 3	Accused Products
<p>3. The charge pump circuit of claim 2, wherein the load selector means further includes a maximum ripple on the target output selector means for adding a load, whenever a maximum ripple on the target output voltage (Vcfrb) greater than the reference voltage (Vref) then the maximum ripple on the target output selector means adds additional loads until the Vcfrb voltage is</p>	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 2, wherein the load selector means further includes a maximum ripple on the target output selector means for adding a load, and whenever a maximum ripple on the target output voltage (Vcfrb) greater than the reference voltage (Vref) then the maximum ripple on the target output selector means adds additional loads until the Vcfrb voltage is less than or equal to the reference voltage (Vref).</p> <p><i>See evidence and explanation for claim element [1a] and claim 2, supra.</i></p>

Claim 3	Accused Products
less than or equal to the reference voltage (V_{ref}).	

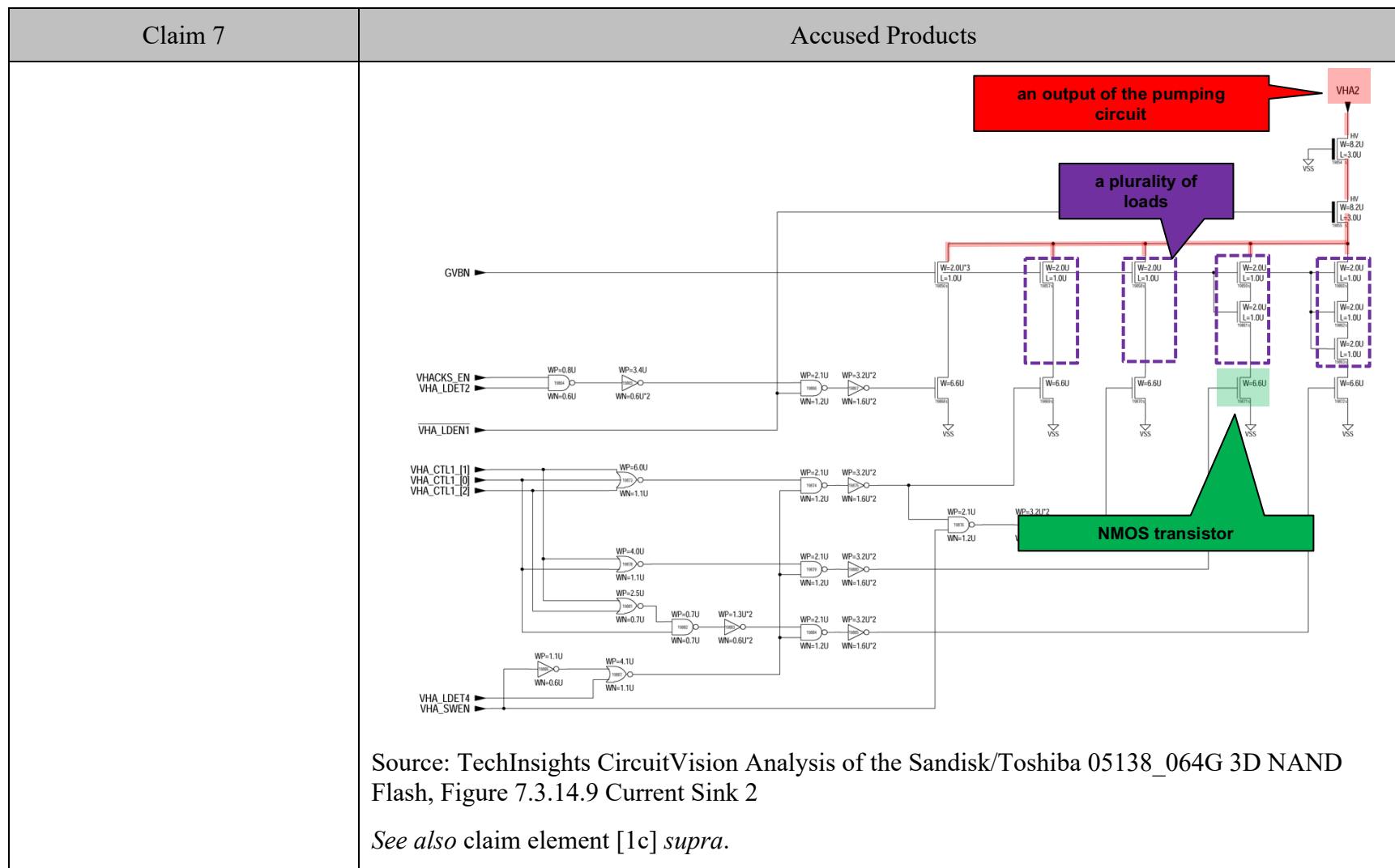
Claim 6

Claim 6	Accused Products
6. The charge pump circuit of claim 1, wherein the load selector means is a plurality of switches, one switch for each of said loads, each switch having a first terminal, a second terminal, and an enable terminal, the switch being coupled in series with each load, the first terminal of the switch being coupled to the output pump and the second terminal of the switch is coupled to each load.	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 1, wherein the load selector means is a plurality of switches, one switch for each of said loads, each switch having a first terminal, a second terminal, and an enable terminal, the switch being coupled in series with each load, the first terminal of the switch being coupled to the output pump and the second terminal of the switch is coupled to each load.</p> <p><i>See, e.g.:</i></p>



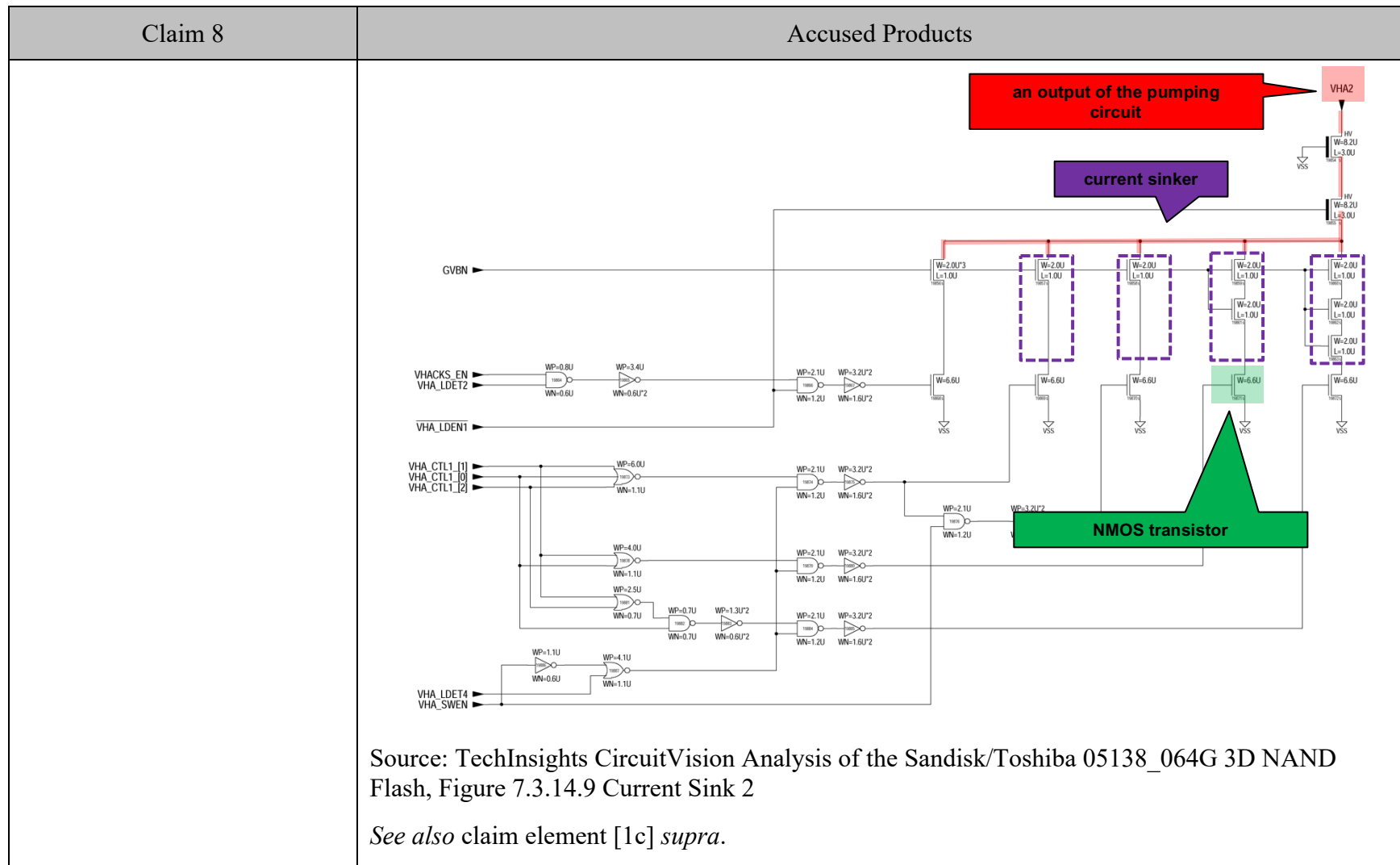
Claim 7

Claim 7	Accused Products
<p>7. The charge pump circuit of claim 1, wherein each load selector means comprises an NMOS transistor having a gate, a drain and a source, the gate of the NMOS load transistor being coupled to an enable signal, the source of the load NMOS load transistor being coupled to an electrical ground, and the drain being coupled to a load.</p>	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 1, wherein each load selector means comprises an NMOS transistor having a gate, a drain and a source, the gate of the NMOS load transistor being coupled to an enable signal, the source of the load NMOS load transistor being coupled to an electrical ground, and the drain being coupled to a load.</p> <p><i>See, e.g.:</i></p>



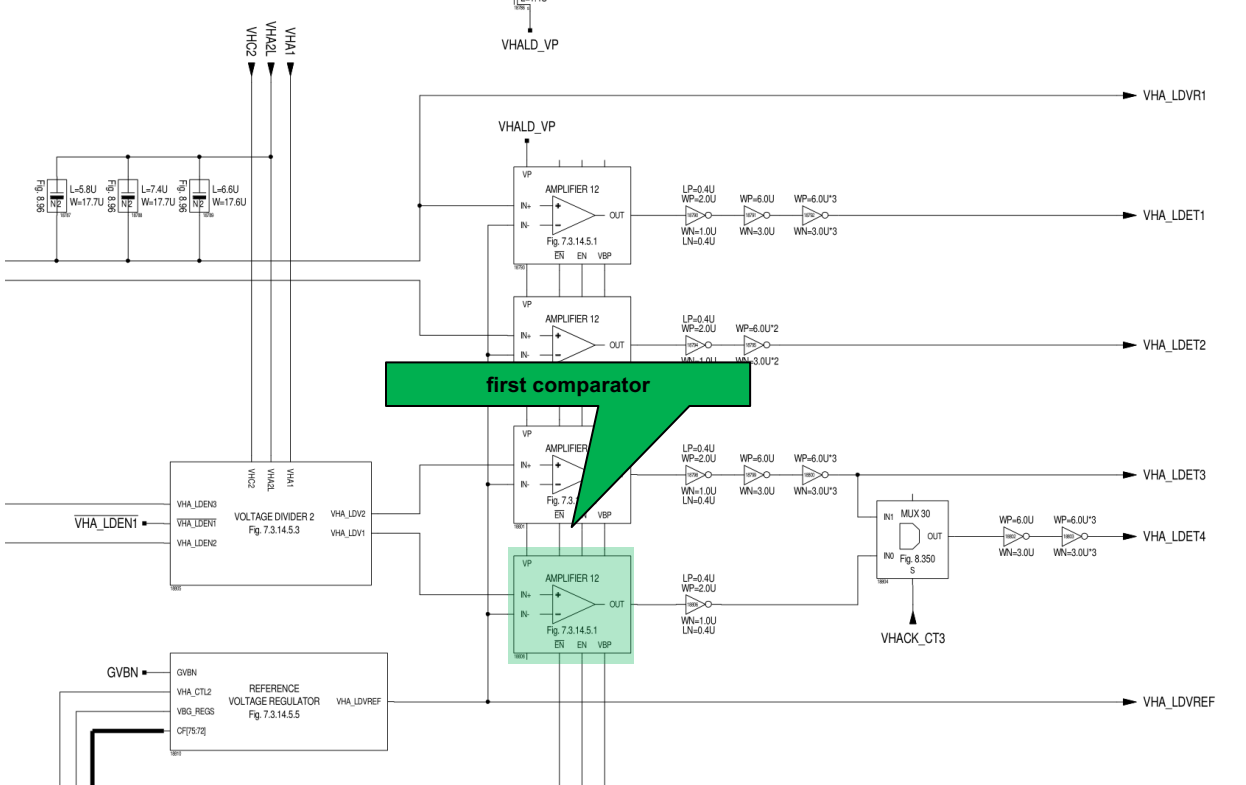
Claim 8

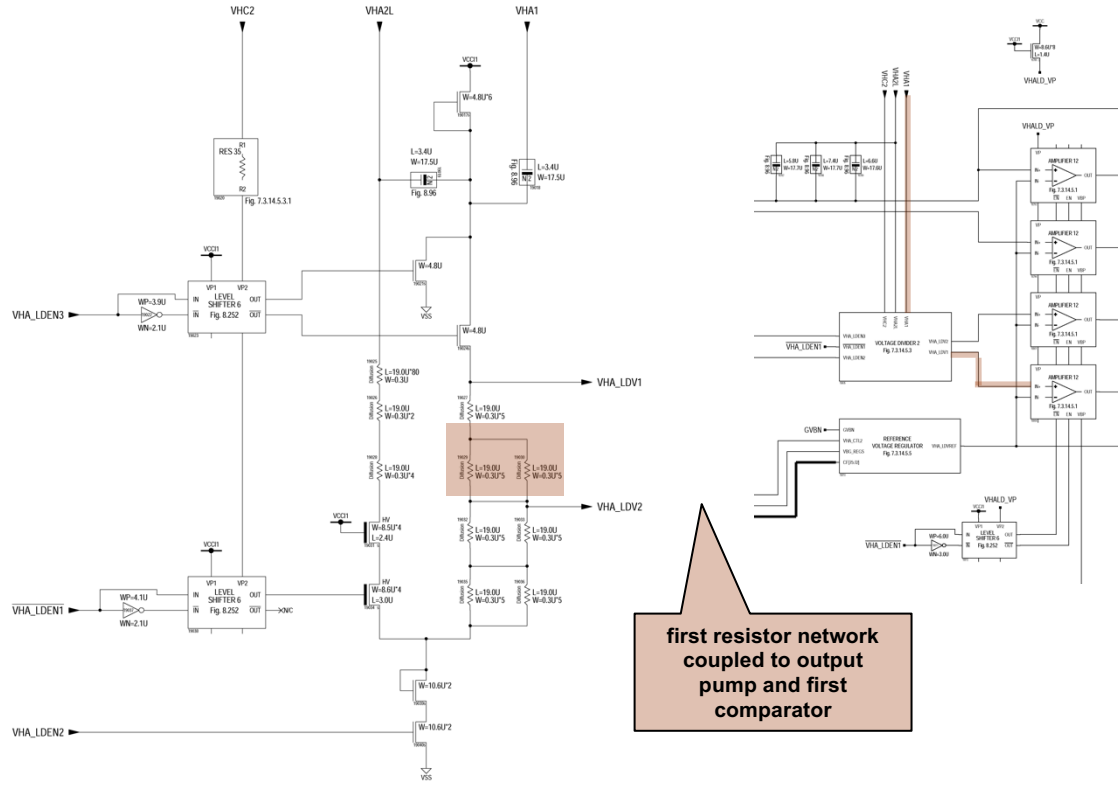
Claim 8	Accused Products
<p>8. The charge pump circuit of claim 7, wherein each load is a capacitor or a current sinker having a first terminal and a second terminal, the first terminal being coupled to the pump voltage and the second terminal being coupled to the drain of the NMOS transistor.</p>	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 7, wherein each load is a capacitor or a current sinker having a first terminal and a second terminal, the first terminal being coupled to the pump voltage and the second terminal being coupled to the drain of the NMOS transistor.</p> <p><i>See, e.g.:</i></p>

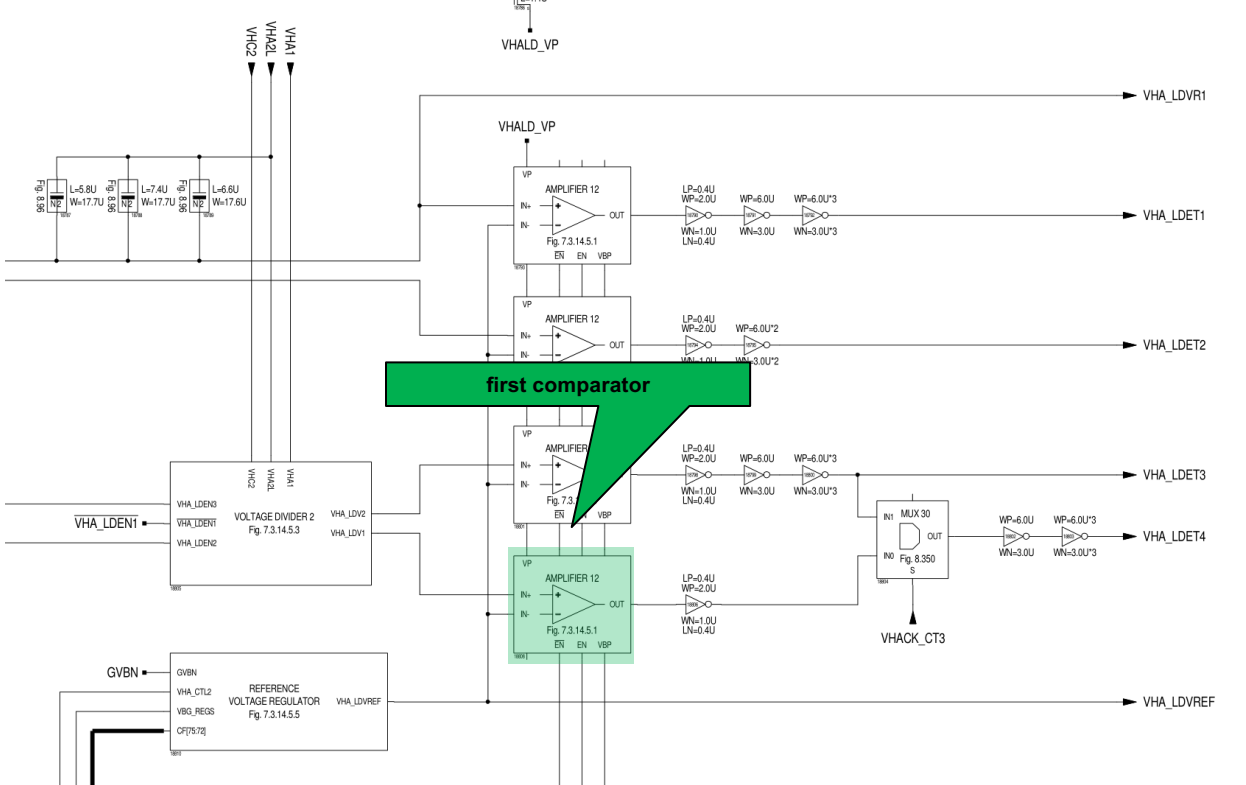


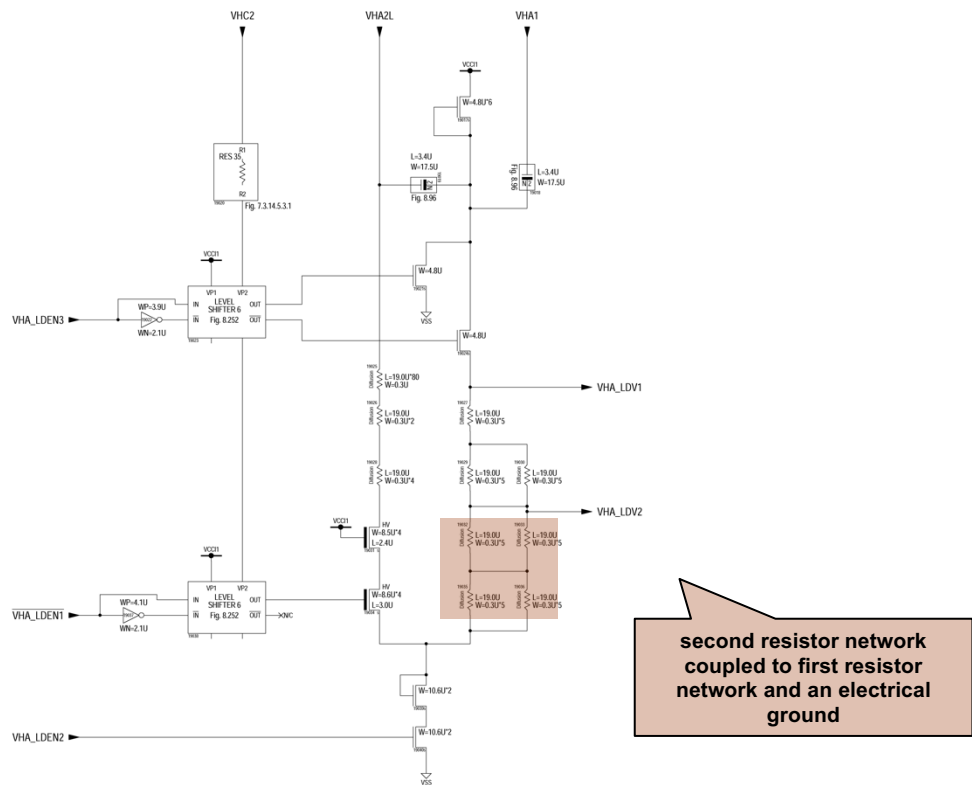
Claim 11

Claim 11	Accused Products
[11pre] 11. The charge pump circuit of claim 2 wherein the target output pump selector comprises:	Each Accused Product includes the charge pump circuit of claim 2. <i>See supra</i> claim 2.
[11a] a) a first comparator having two input terminals, an output terminal and a first enable terminal, one of the two input terminals being connected to the reference voltage (Vref);	Each Accused Product includes a first comparator having two input terminals, an output terminal and a first enable terminal, one of the two input terminals being connected to the reference voltage (Vref). <i>See, e.g.:</i>

Claim 11	Accused Products
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>
<p>[11b] b) a first resistor network having two terminals, the first terminal being coupled to the output pump, the second terminal being coupled to one of the input terminals of the first comparator;</p>	<p>Each Accused Product includes a first resistor network having two terminals, the first terminal being coupled to the output pump, the second terminal being coupled to one of the input terminals of the first comparator.</p> <p><i>See, e.g.:</i></p>

Claim 11	Accused Products
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5.3 Voltage Divider 2; Figure 7.3.14.5 Level Detector 6</p>

Claim 11	Accused Products
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>
<p>[11c] c) a second resistor network having two terminals, the first terminal being coupled to the second terminal of the first resistor network, and the second terminal of the second resistor network being</p>	<p>Each Accused Product includes a second resistor network having two terminals, the first terminal being coupled to the second terminal of the first resistor network, and the second terminal of the second resistor network being coupled to an electrical ground.</p> <p><i>See, e.g.:</i></p>

Claim 11	Accused Products
coupled to an electrical ground; and	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5.3 Voltage Divider 2</p>
[11d] d) a reference voltage source (Vref) coupled to one of the input terminals of the first comparator.	<p>Each Accused Product includes a reference voltage source (Vref) coupled to one of the input terminals of the first comparator.</p> <p><i>See, e.g.:</i></p>

Claim 11	Accused Products
	<p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>